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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/022,123 | 12/13/2001 | Sifen Luo | US 010624 | 2515 |

24737 7590 09/05/2003

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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| EXAMINER | |
|---|---|
| NGUYEN, LINH V | |
| **ART UNIT** | **PAPER NUMBER** |
| 2819 | |

DATE MAILED: 09/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 10/022,123 | Applicant(s) LUO ET AL. | |
|---|---|---|---|
| | Examiner Linh V Nguyen | Art Unit 2819 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *7/08/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *03/29/02* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

1. Claims 1 - 26, are rejected under 35 U.S.C. 102(e) as being anticipated by Shinjo et al. Pub. No.: 2003/0048135 A1.

Regarding to claim 1, Figs. 2 – 5, of Shinjo et al. disclose an multi-stage RF power amplifier circuit having at least an input stage (1) and output stage (3) comprising: sensing a collector current in an input stage transistor (33); feeding a current equal or proportional to said input stage transistor collector current (collector current of 33) to an output stage bias circuit (26) to boost the bias of an output stage (see 2); wherein the input stage transistor is operated in a class AB mode (See Page 4 paragraph [0053]), and said output stage is fed through a matching network ( 11, 14 ).

Regarding to claim 2, wherein the input stage transistor collector current is sensed and fed to the output stage bias circuit via a current mirror (Figs. 3 and 4).

Regarding to claim 3, wherein one transistor comprising said current mirror is connected in series with a transistor that itself forms a second current mirror with the input stage transistor (Figs. 3 and 4).

Regarding to claim 4, wherein the amplifier circuit comprises plural bipolar junction transistors (Figs 3, 4, 5).

Regarding to claim 5, wherein the amplifier circuit comprises plural field effect transistors (Fig. 2).

Regarding to claim 6, wherein the amplifier circuit comprises a combination of BJTs and FETs (Figs. 2 – 5).

Regarding to claim 7, Figs. 2 – 6 of Shinjo et al. disclose a multi-stage power amplifier circuit comprising: an input stage (1); an output stage (Fig. 2) with a biasing circuit (26); and a current mirror, which senses an input signal current in said input stages (Fig. 3) and feeds a current proportional to said input signal current to said output stage biasing circuit ( See Figs 3 – 5).

Regarding to claim 8, wherein said current mirror includes at least one BJT (Figs. 3 - 5).

Regarding to claim 9, wherein said current mirror includes at least one FET (Figs. 2).

Regarding to claim 10, wherein said transistor comprised within said circuit includes both BJTs and FETs (Figs 2 – 6).

Regarding to claims 11 – 20, Figs. 2 – 6 of Shinjo et al. as applied to claims 1 – 10 above, disclosed every aspect of applicant claims invention.

Regarding to claim 21, Figs. 2 – 6 of Shinjo et al. disclose a bias boosting sub-circuit (26) for a multi-stage power amplifier circuit (Fig. 2), said multistage power amplifier comprising at least an input stage (1) and an output stage (3), said sub-circuit comprising: two matched BJTs in a first current mirror (Fig. 3 [32,33]), wherein the first current mirror senses a collector current of an amplifying transistor (112) in the input stage, and feeds an equal or proportional current to a bias circuit (Fig. 4) of the output stage (Fig. 2).

Regarding to claim 22, wherein one of the transistors of the first current mirror is connected in series with a third transistor, said third transistor itself forming a second current mirror with the input stage-amplifying transistor (Fig. 4 [41,42]).

Regarding to claim 23, wherein one transistor of the first current mirror comprises two matched PNP BJTs, and the second current mirror comprises two matched NPN BJTs (Figs. 3 – 5).

Regarding to claim 24, where one transistor of the first current mirror has its collector connected to a collector of the third transistor (Figs 3 and 4).

Regarding to claim 25, the subcircuit further transistors and wherein a collector current mirror and is connected to a collector of an NPN transistor in the output stage (Fig. 4 – 5).

Regarding to claim 26, wherein the NPN transistor is a current mirror (Fig. 5).

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (703) 305-1934. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LVN

August 25, 2003

Michael J. Tokar

Michael Tokar
Supervisory Patent Examiner
Technology Center 2800